REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-5 remain in the application. None of the claims have been amended.

On page 2 of the above-identified Office action, the Examiner rejected claims 1-6 under 35 U.S.C. 102(e) as being anticipated by Mori et al. (US 6,335,570 B2).

Applicant respectfully draws the Examiner's attention to the fact that Mori et al. has an effective filing date of April 20, 1999. As set forth in the declaration of record, the instant application claims the priority, under 35 U.S.C. § 119, of German patent application 198 43 624.6, filed September 23, 1998. Pursuant to 35 U.S.C. §§ 119, 120 and 363, applicant is entitled to the priority date of the German application. Thus, the instant application predates the Mori reference by seven months and, accordingly, Mori et al. is unavailable as prior art.

Applicant acknowledges that perfection of priority can only be obtained by filing a certified English translation of the German priority application. 35 U.S.C. § 119. Enclosed herewith is a certified English translation of German

application 198 43 624.6. A certified copy of the German application was filed in parent application No. 09/816,923, now U.S. Patent No. 6,828,680 B2. Accordingly, applicant respectfully believes that priority has been perfected and that the Mori et al. reference is unavailable as prior art.

In view of the foregoing, the Section 102 rejection on pages 2-4 of the Office action is now moot.

Similarly, the rejection of claims 1-3 as being obvious under 35 U.S.C. § 103 over a combination of Zhao et al. (US 6,100,184) and Mori et al. is moot as well.

The only remaining issue, then, is the rejection of claim 6 as being obvious over a combination of Zhao et al. (US 6,100,184, hereinafter "Zhao") with Jain (US 5,821,168) under 35 U.S.C. § 103. We respectfully traverse.

The rejection is, in fact, not tenable. The combination of the two reference teachings is based on factual error and on legal error. The Examiner is requested to reconsider. We do not entirely disagree with the Examiner's summary of the primary reference Zhao. In response, however, we must stress the fact that applicant's claims define a process sequence in which

spacers are formed first, and the contact hole is subsequently opened down to the first conductive structure.

This, of course, is exactly the primary reason why the spacers (11') are provided. During the etching of the layer 7 down to the conductor 6, some material from the conductor 6 may be lifted and removed through the opening 10. Were it not for the spacers 11', the conductor material may cling to the sidewalls and then diffuse into the second insulating layer 8. The spacers 11' protect against such deposition and diffusion which, of course, would destroy or severely impair the insulating effect of the layer 8.

The reference Zhao teaches: (1) etching the via 24 down to the layer 13; (2) etching the bottom of the via 24 to expose the conductive material 10; (3) conformally depositing (i.e., encapsulating) a barrier layer 28; and (4) filling the via with conductive material 29. The barrier layer 28 is typically a metal. Col. 8, lines 22-23. Its purpose is to protect the low dielectric constant materials of the layers 14 and 18 against the conductor in the via (copper or aluminum). Col. 8, lines 23-26.

Most notably with regard to the claimed invention, the via 24 is etched down through the layer 13 without any protection on

the sidewalls, i.e., the exposed walls in the layer 14. In fact, such "protection" is neither necessary in the context of Zhao, nor is it suggested.

The secondary reference Jain does not modify Zhao to render obvious the claimed invention. Firstly, we cannot find any suggestion in the art why Zhao should be so modified. The primary reference teaching appears to be properly functional without sidewall spacers. Secondly, the purpose of sidewall protection provided by Jain has absolutely nothing in common with the claimed invention.

Jain first provides a diffusion barrier 56 (by either converting the exposed oxide portions 52 to silicon oxynitride, col. 3, lines 33-35, or by converting portions of the layer 30 into diffusion barrier portions, col. 4, lines 57-60) and then places a silicon adhesion layer 58 on the nitrided oxide portions 56, col. 3, lines 55-56. There is simply no danger, in the context of Jain, that "material removed at the surface of the first conductive structure" may deposit on the sidewalls of the via. See specification, page 14, bottom.

Furthermore, Jain etches all the way down to the conductor 28 prior to forming the barrier layer 56. Fig. 4. In fact, the

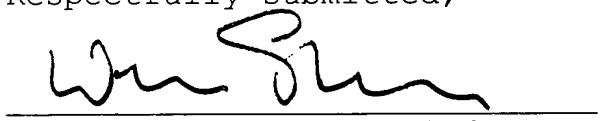
insulator 52 (including the layers 48, 26, 50, 54) is first patterned and the exposed oxide surfaces are then converted to the barrier layer 56 "[A]fter patterning the insulating layer 52." Col. 3, lines 31-33. This sequence is similar to the Zhao sequence and it is different from the claimed sequence.

In view of the foregoing, the rejection of claim 1 as being obvious over Zhao and Jain is not warranted. None of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 6. All of the claims are, therefore, patentable over the art of record.

In view of the foregoing, reconsideration and allowance of claims 1-6 are solicited.

If an extension of time for this paper is required, petition for extension is herewith made.

Respectfully submitted,



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June 8, 2005

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